MicroBooNE

F. Lanni for the MicroBooNE collaboration

Outline:

- The experiment proposal, the context and the physics case
- How microBooNE fits into the more general R&D program on LArTPC
- Review of the R&D staged programs in microBooNE: issues and open questions
  - ✓ Phase I R&D: microBooNE related developments and optimizations
  - ✓ Phase 2 R&D: longer term studies. Emphasis on readout aspects

The MicroBooNE proposal

31 scientists, 7 institutions

- Proposal submitted to the PAC in Nov 07
- Revised proposal (addendum) reviewed at the Mar 08 PAC meeting
- Technical scaling and R&D aspects to be reviewed at the meeting in June

MicroBooNE Proposal Addendum

March 3, 2008

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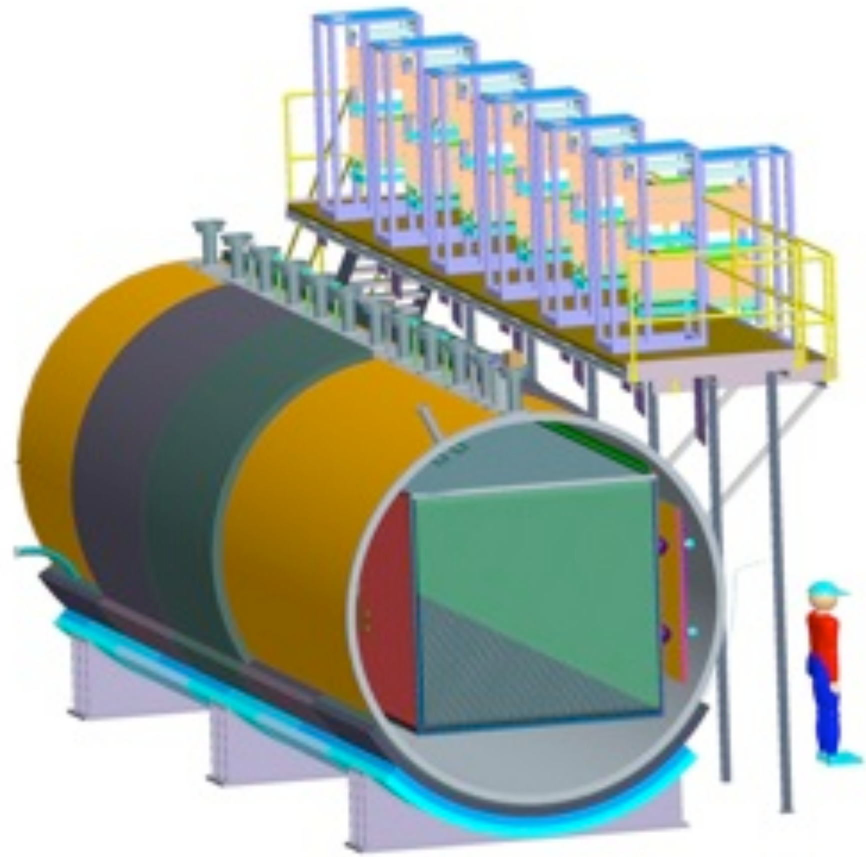
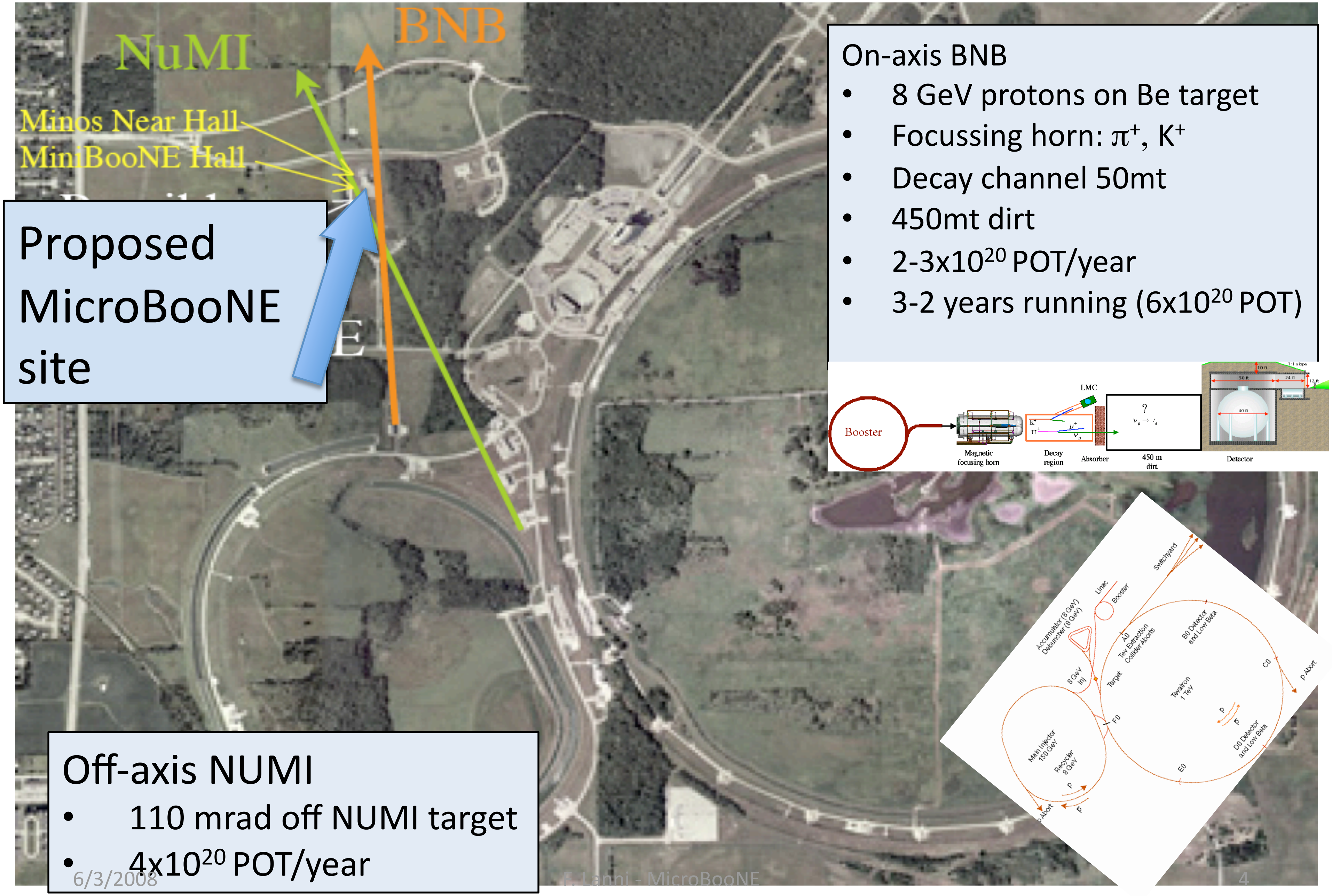
Detector Overview

- LAr TPC
  - 70 ton fiducial volume
  - 2.5mt drift @ 500V/cm
- 3 Readout planes
  - 2 induction planes (U,V at ±60° from vertical, 5m max. length)
  - 1 collection plane (vertical wires, 2.5m long)
- 30 PMT for T0 determination
- Single vessel containment
  - Evacuable
  - Thermal insulation through multi-layer glass foams
  - No expansion vessel (8% ullage)
- Readout based on "cold" preamplifiers
  - JFET based discrete
  - 10,000 channels
  - Warm Feedthroughs
- Bi-phase purification system (not discussed here, see Stephen talk)



Experimental Program

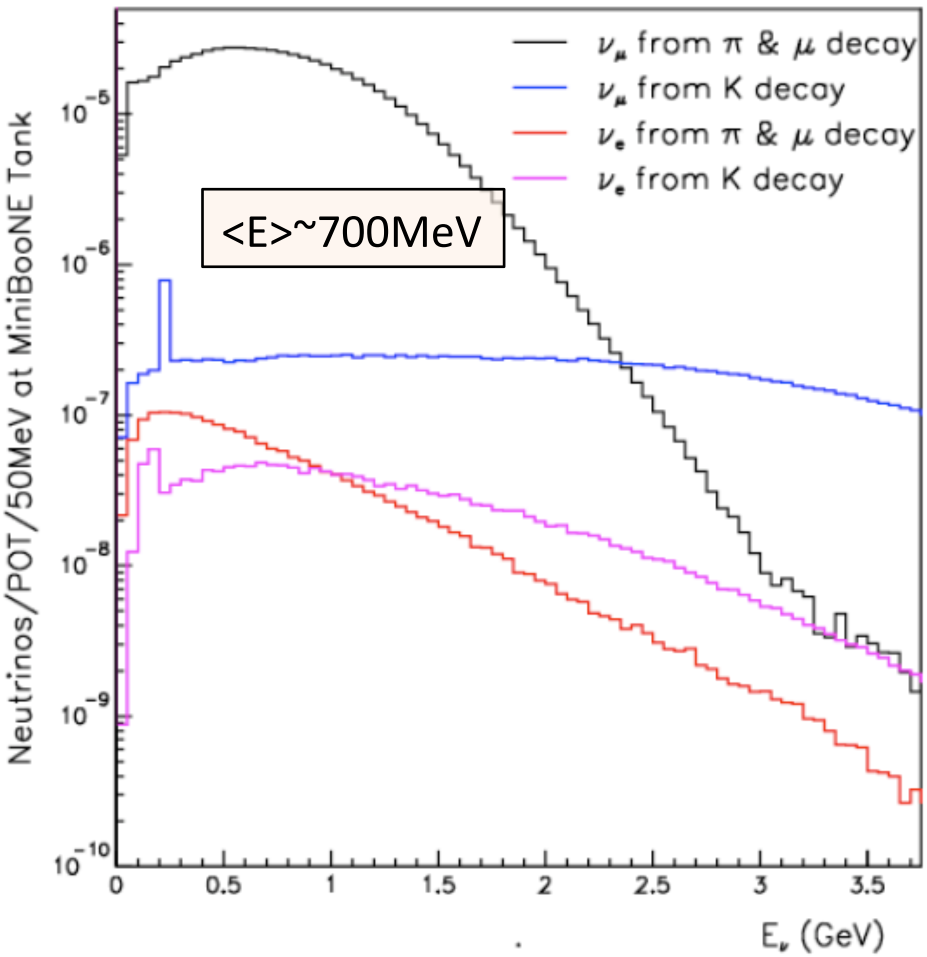


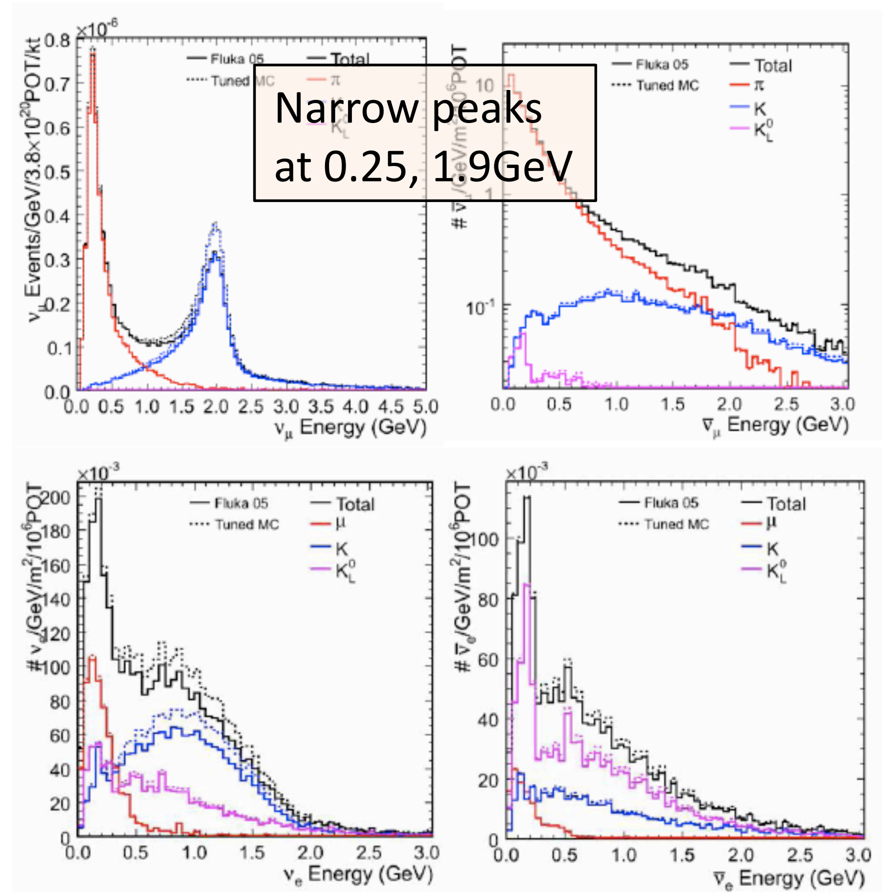
Proposed MicroBooNE site

On-axis BNB
- 8 GeV protons on Be target
- Focussing horn: π^+, K^+
- Decay channel 50mt
- 450mt dirt
- 2-3x10^{20} POT/year
- 3-2 years running (6x10^{20} POT)

Off-axis NUMI
- 110 mrad off NUMI target
- 4x10^{20} POT/year

Experimental Program





On-axis BNB

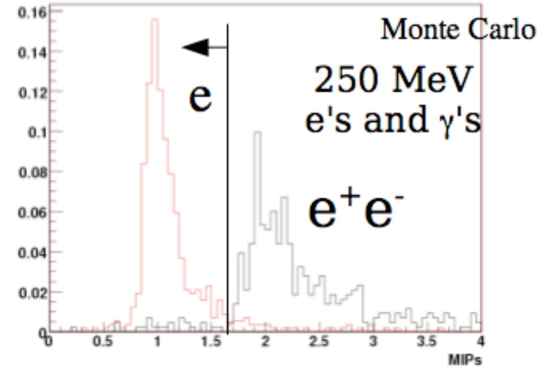
- Flux from miniBooNE
- Events: 100k total, 39k CCQE ν_μ, 8k NCπ^o, 250 ν_e CCQE from intrinsic ν_e

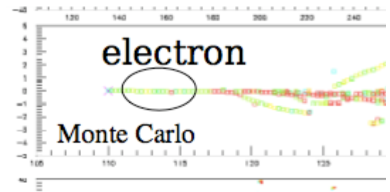
Off-axis NUMI

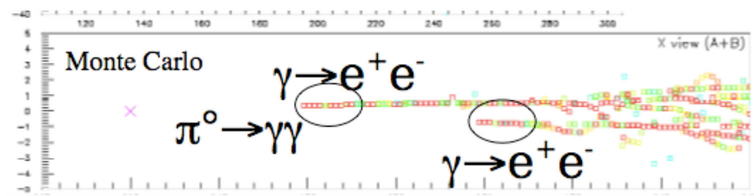
- 21k CC ν_μ, 7k NC, 1.7k CC ν_e [LE configuration]
- Fluka2005 calc. (solid)/Tuned w. MINOS data (dashed)

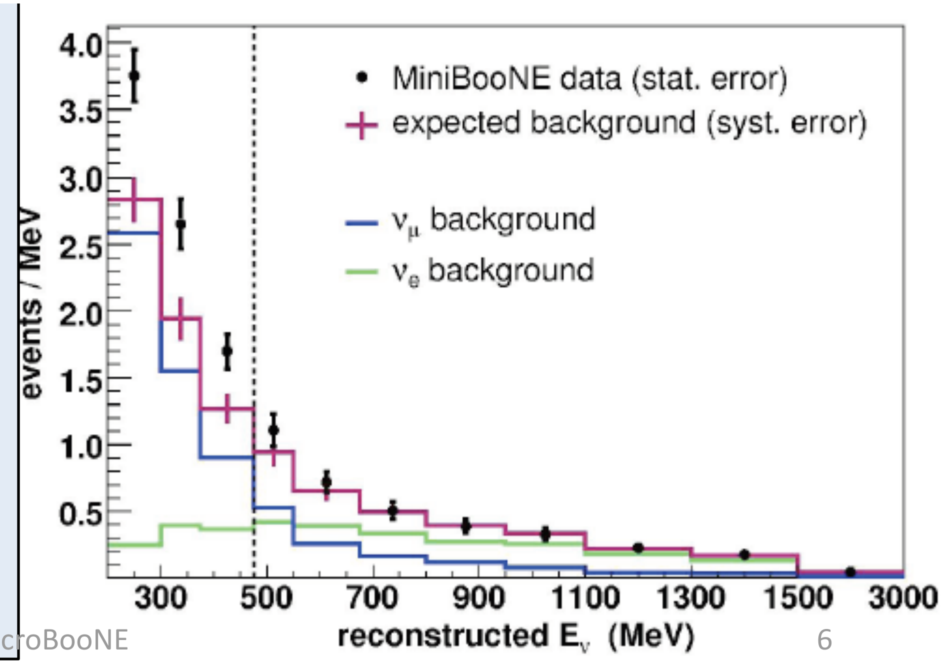
Physics Motivations

- Uniqueness in the e/γ/π^o tag
  - A first time (almost) in neutrino oscillation experiment
  - Particularly at low energy thanks to low sensitivity (down to MeV scale) and high resolution
- Precision measurements of "golden" ν_μ CCQ channel:
  - 15k events fully contained
  - Axial mass parameter M_A ,(recent results from K2K…)
- Possibility of CCQE measurements from intrinsic ν_e
- Rare channel measurements (Δ -> Nγ, K production
- Background for oscillation searches: NCπ^o, photonuclear events
- Low Energy Phenomena:
  - miniBooNE observes low energy ν_e excess on the BNB data (3.7σ effect for energies 300-475MeV)
  - If neutrinos with powerful LArTPC the significance would boost to 9σ in the 200-475MeV bin
  - Anomalous γ-production [in the SM] (Harvey,Hill,Hill 2006)









MicroBooNE in the R&D program

Detector Physics R&D:

- Full scale experiment. Detector operations and analysis of real data provides best tools to understand strengths and shortcomings:

ν–Ar Cross Section Measurements

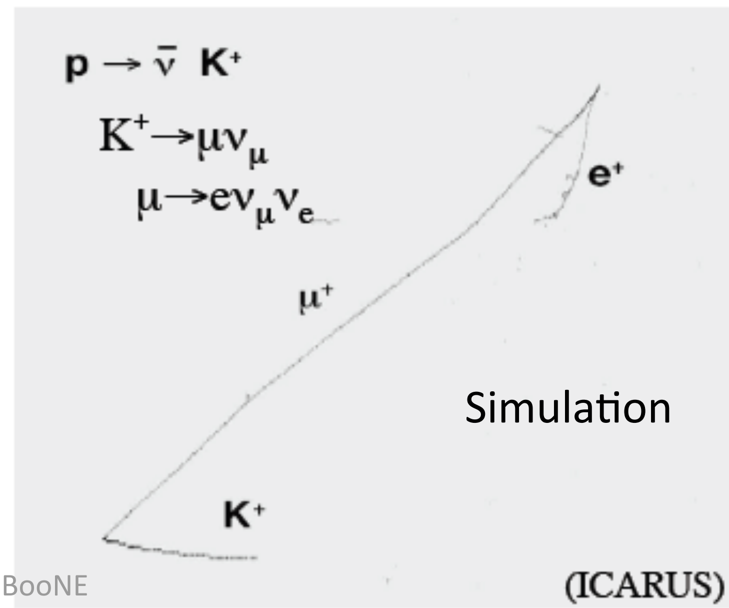
- Relevant for future oscillation experiments (Physics R&D)
- Expect ~100k events from BNB (6E20 POT), ~60k events from NOA [LE configuration] (8E20 POT)

Muon Momentum Determination

- dE/dx + range
- Multiple Scattering
- Momentum balance (recoil proton)

Studies for p decay sensitivity

- Extend reach particularly trough νK channels (>90% eff. Vs. 17% in WC)
- Expected 500 kaons from BNB
- K-id study through dE/dx
- Background rejection



MicroBooNE in the R&D program

MicroBooNE R&D program staged into two overlapping phases

Tuned for optimal combination of R&D for large scale detectors and physics goals

Phase-I

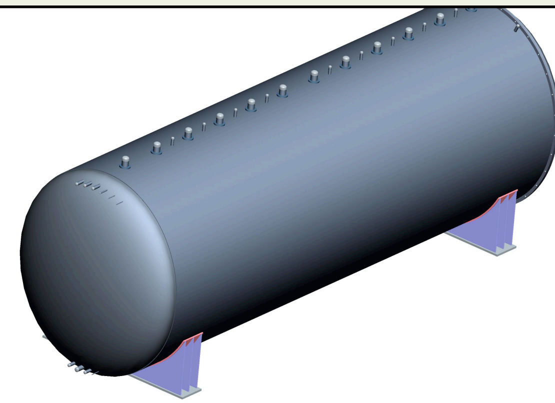
- Design aspects specific to the MicroBooNE project
- Including changes and evolution of the detector design (see Addendum submitted for the PAC spring meeting)
- With no doubts it benefits of many years of R&D by ICARUS mainly
- Cryostat, FT
- TPC detectors: wires
- PMT readout and t0 determination
- JFET based cold preamplifiers

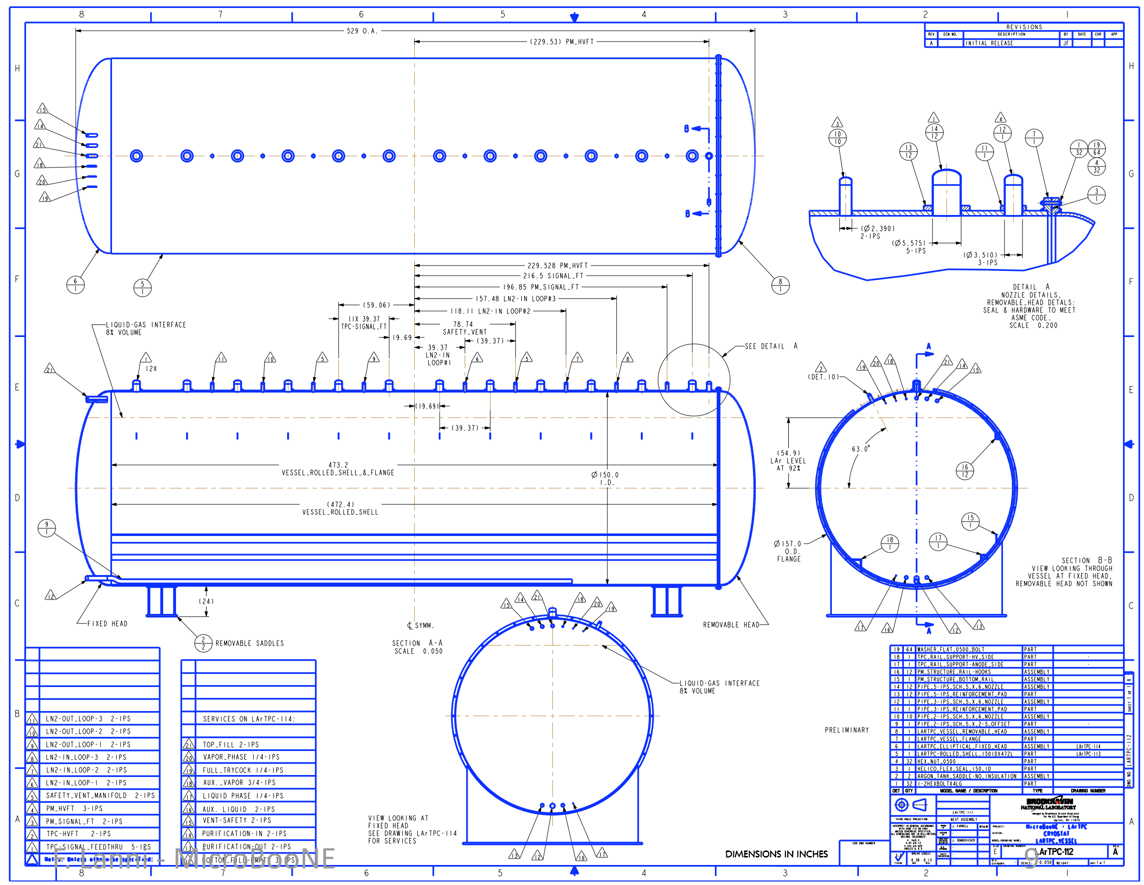
Phase-II

- Longer term studies for the next stages in the LArTPC R&D program
  - See David and Gina talks
- Purification/ purity in large un-evacuated cryostats (Stephen)
- Development of a fully integrated ASIC operating at cryogenic temperatures
- Detector design studies for large volume detectors underground (David)

Phase-I: Cryostat

- Single vessel containment
- Evacuable
- MAWP 1.8 bara
- Austenitic SS Type 304 1” thick
- OD=152” (3.8mt)
- Length ~15m
- Max. standard size for transport over the road
- Constructed to the latest ASME Boiler Code and U stamped
- 2 domed ends:
  - 1 Welded
  - 2nd flanged and bolted (for installation and detector access)
  - Helicoflex seal (low pressure so Indium or GoreTex would also work)
- 2 cradles matched to the outer diameter to support total load (~230 metric tons)
- 16” nozzles at vertical position for services and signal/HV FTs

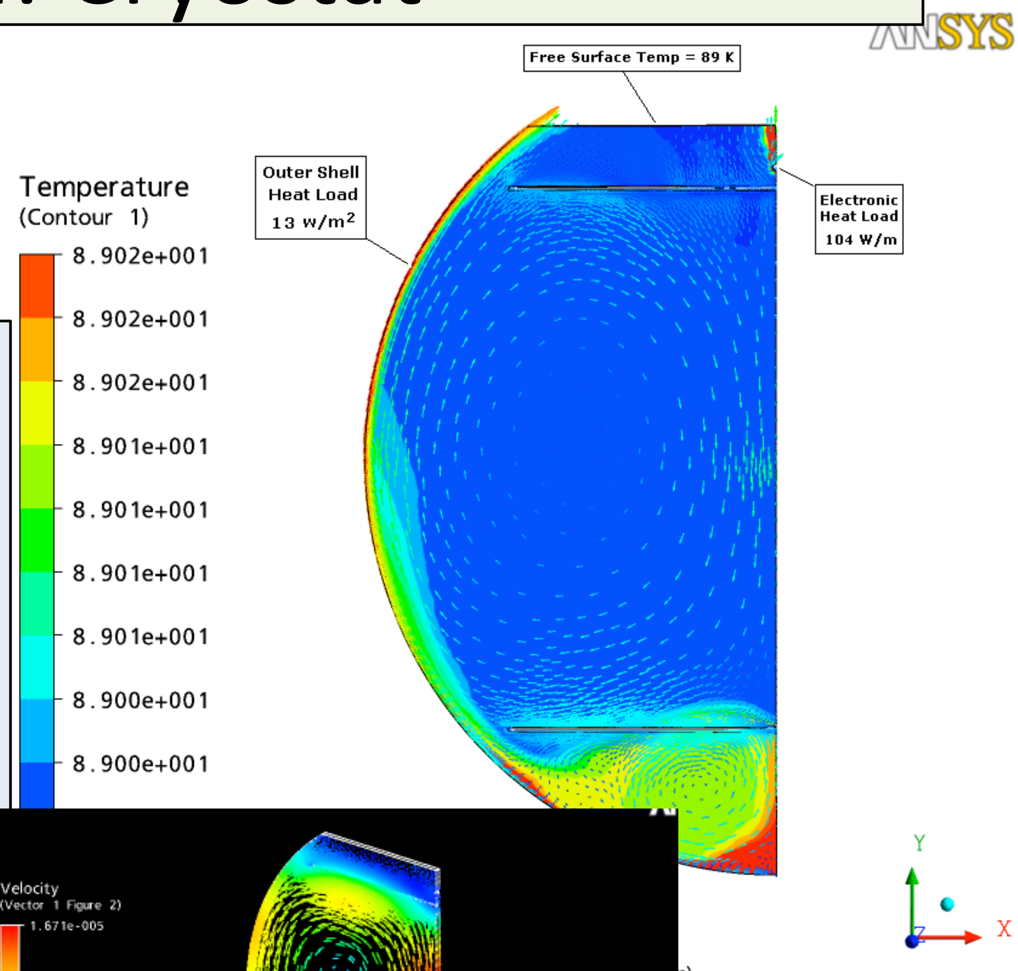


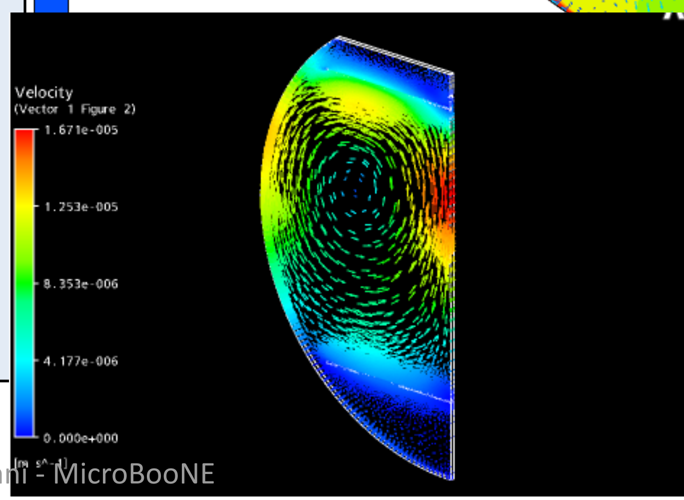


Phase-I: Cryostat

- Heat Leak Estimate through the walls
  - Aassuming 16” glass foam:
  - 3.4kW (13W/msq)

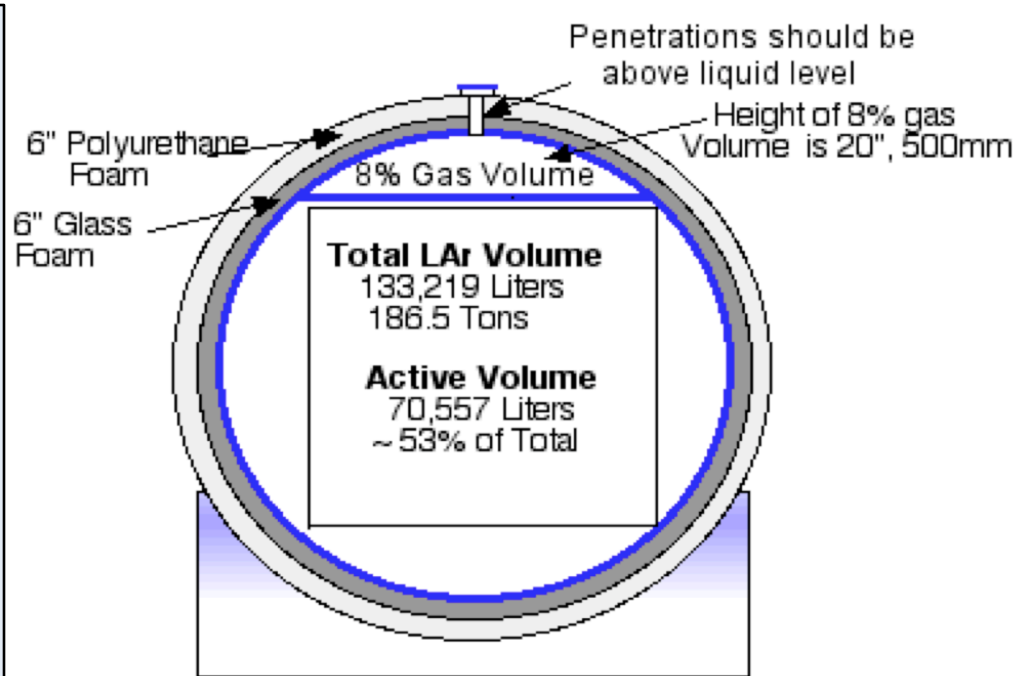
- Preliminary simulations by Rich Schmitt
- Mirror simmetry
- Subcooling L/G surface 89K
- Convection established minimizing temperature gradient to <<0.1K
  - T-sensors
  - Can we extrapolate T-gradients from muon tracks?
- Convection flow remains low





Phase-I: Cryostat

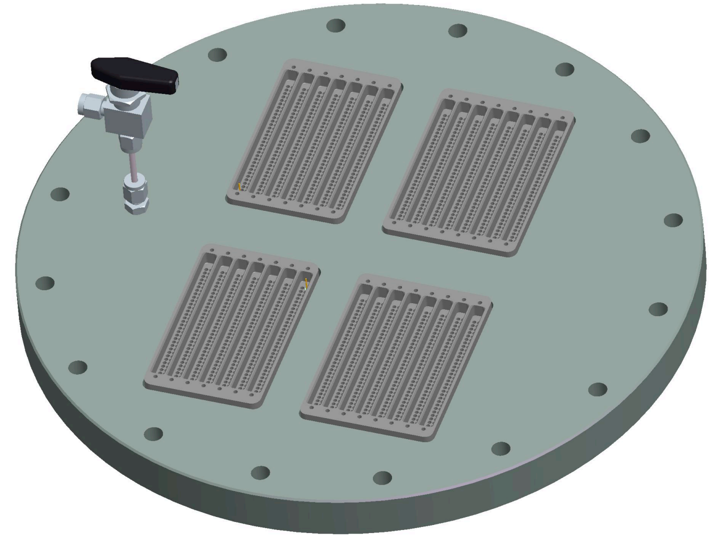
- Design evolution over the last 10 months
- No expansion vessel
  - 8% Ullage
- Single vessel containment. Thermal insulation through 16” foam
  - Perlite, Glass Foam



- Glass foam:
  - No water absorption
  - >90psi compressive strength
  - Costs

Phase-I: Feedthroughs

- "Warm" FT
- Cables from the cold-electronics in the GAr to a warm flange housing pin carriers
- Revised Atlas design: pin carrier rows welded on Conflat@ flange
- Manuf. and welding process validation for Atlas on pin carriers:
  - Speciment bolted to another flange w. tube welded for fluid access
  - Hydrostatically pressurized up to 51.7 bars (10 minutes)
  - Pin carrier leak check in vacuum at 10-5 torr
  - Leak Rate <1e-9 std. cc/sec He@1 bar difference
- Special welding procedure developed for Atlas.
  - Section after welding for micrographic inspection
- Production tests: thermal cycles and vacuum leak test before/after welding on flange



- Carriers made of AISI 304L SS
- Special Glass as sealant insulator
- Soft metal pins to match CTE of the glass
- Pins mounted on jig while glass pouring process (Glasseal ©]
- Pin and wells plated
  - 50uin Au over 50 in Ni
- Insulation Resistance: 2GOhm (@500VDC)
- Dielectric Withstand: 600VAC RMS 60Hz

Phase-I: Light Readout

- LAr is an excellent scintillator…
  - In the VUV: 128nm
  - De-excitation of two molecular states ($^1\Sigma^+_u$, $^3\Sigma^+_u$) to the ground-state, yielding a faster and a slower component
  - **Excitation luminiscence**: Direct excitation of an Ar atom and formation of an excimer (two or three body process)

$$\mathrm{Ar}^* + \mathrm{Ar} \rightarrow \mathrm{Ar}_2^* \rightarrow 2\mathrm{Ar} + \gamma\ (128\ \mathrm{nm})$$

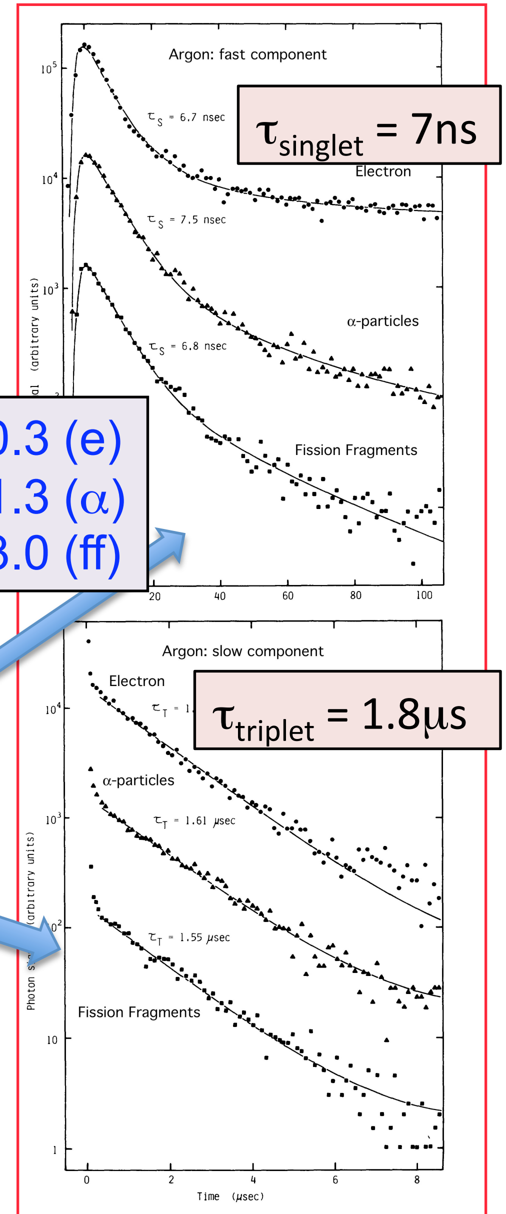
  - **Recombination luminiscence**: recombination of thermalized electrons with a ionized molecule Ar^+_2

$$\mathrm{Ar}^+ + \mathrm{Ar} \rightarrow \mathrm{Ar}_2^+ + \mathrm{e} \rightarrow \mathrm{Ar}_2^* \rightarrow 2\mathrm{Ar} + \gamma\,(128\ \mathrm{nm})$$

    - Depends on drifting electric field and ionization density

- Yield: W_{sci}~25eV (ICARUS – NIM A432 (1999), pp. 240-248)
  - **50% of energy loss goes in light!!! ➔ 20-50k photons/MeV**
- Emission/Absorption spectra no overlapping (almost):
  - **Attenuation Length: ~1mt** (ICARUS NIM A505 (2003), pp. 89)

I_s/I_t = 0.3 (e)
I_s/I_t = 1.3 (α)
I_s/I_t = 3.0 (ff)



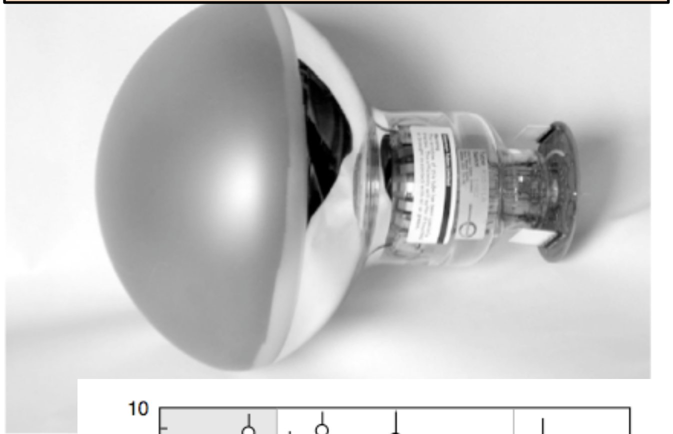
Phase-I: Light Readout

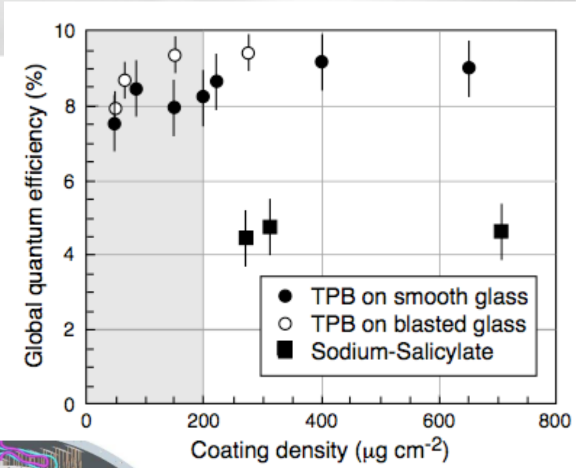
From ICARUS – NIM A505 (2003)

PMT to collect VUV light for T0 determination:

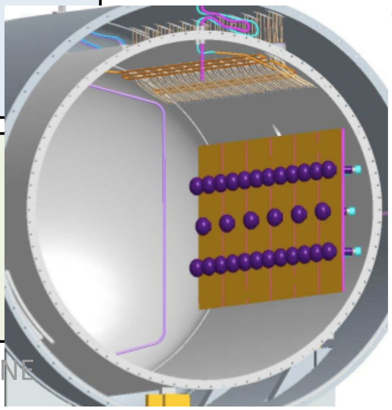
- Cryogenic operations:
  - Bialkali photocatodes become resistive at low temperature
  - Pt undercoating allows operations at T=87K
  - PMT gain @87K (5e7) ~20% nominal value at RT
- VUV sensitivity:
  - TPB (tetraphenyl-butadiene) as WL shifter
  - Prepared in a solution w. toluene
  - Applied on glass-surface w. nebulizer (uniformity and fine grained)
  - Thicknesses <200ug/cm don't introduce mechanical instabilities in cryo-liquids
  - Glass sand-blasting makes good adhesion
- QE measurements: 8-10%
  - No angular dependence

8" 9357FLA Electron Tubes PMT



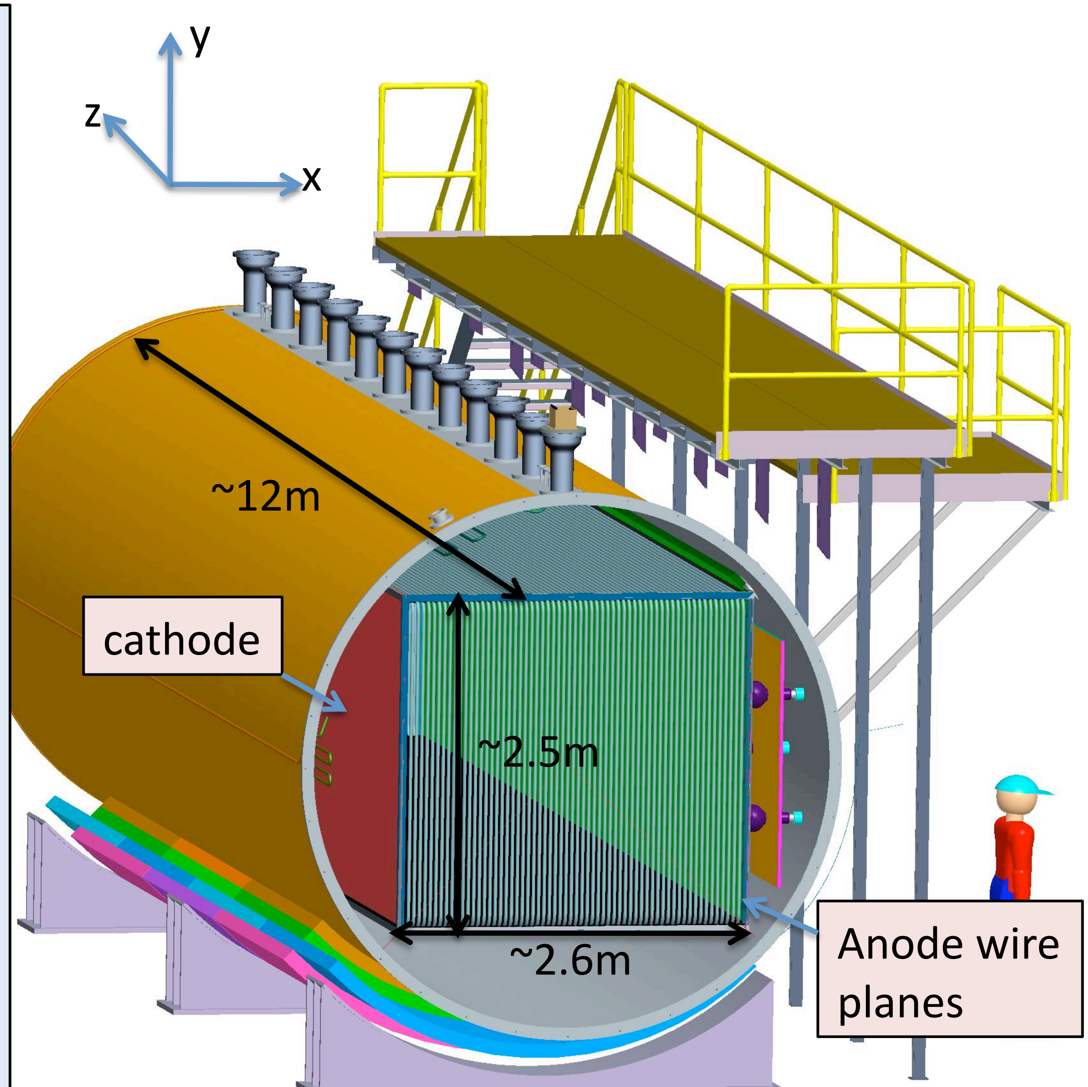


- Array of PMT (30) behind the wire planes
  - Geometry layout to be optimized
  - Mechanical support to be designed

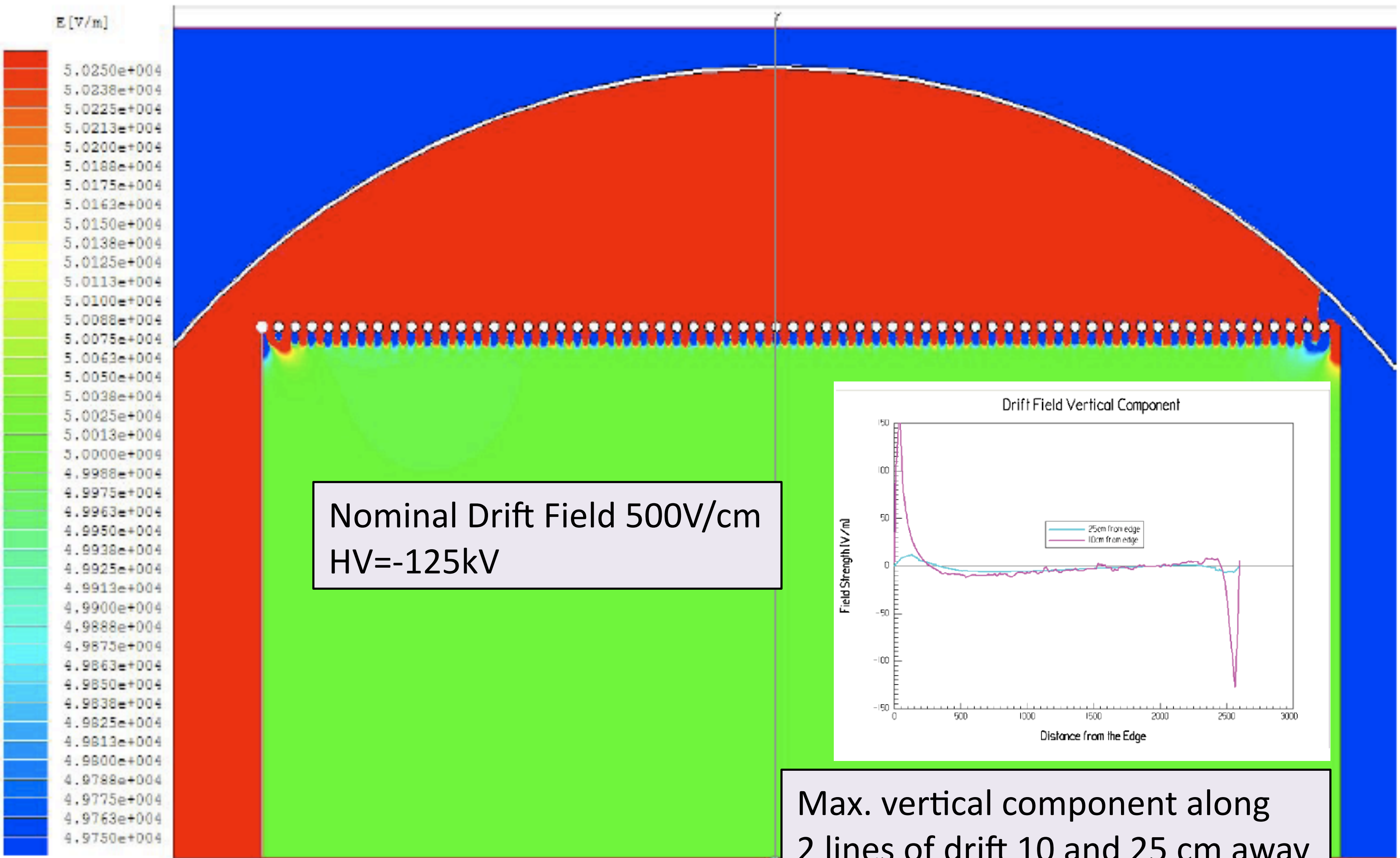


Phase-I: TPC geometry

- TPC volume: 70 ton fiducial, ~170 total
- Slightly off-axis from the cathode size
- Field Shaping Rods around in the yz plane.
  - 25mm diameters
  - 40mm pitch
- 3 wire planes:
  - U,V at ±30^{o} horizontal (z) axis
  - Vertical collection plane
  - Plane distance: 3mm
  - Wire pitch: 3mm



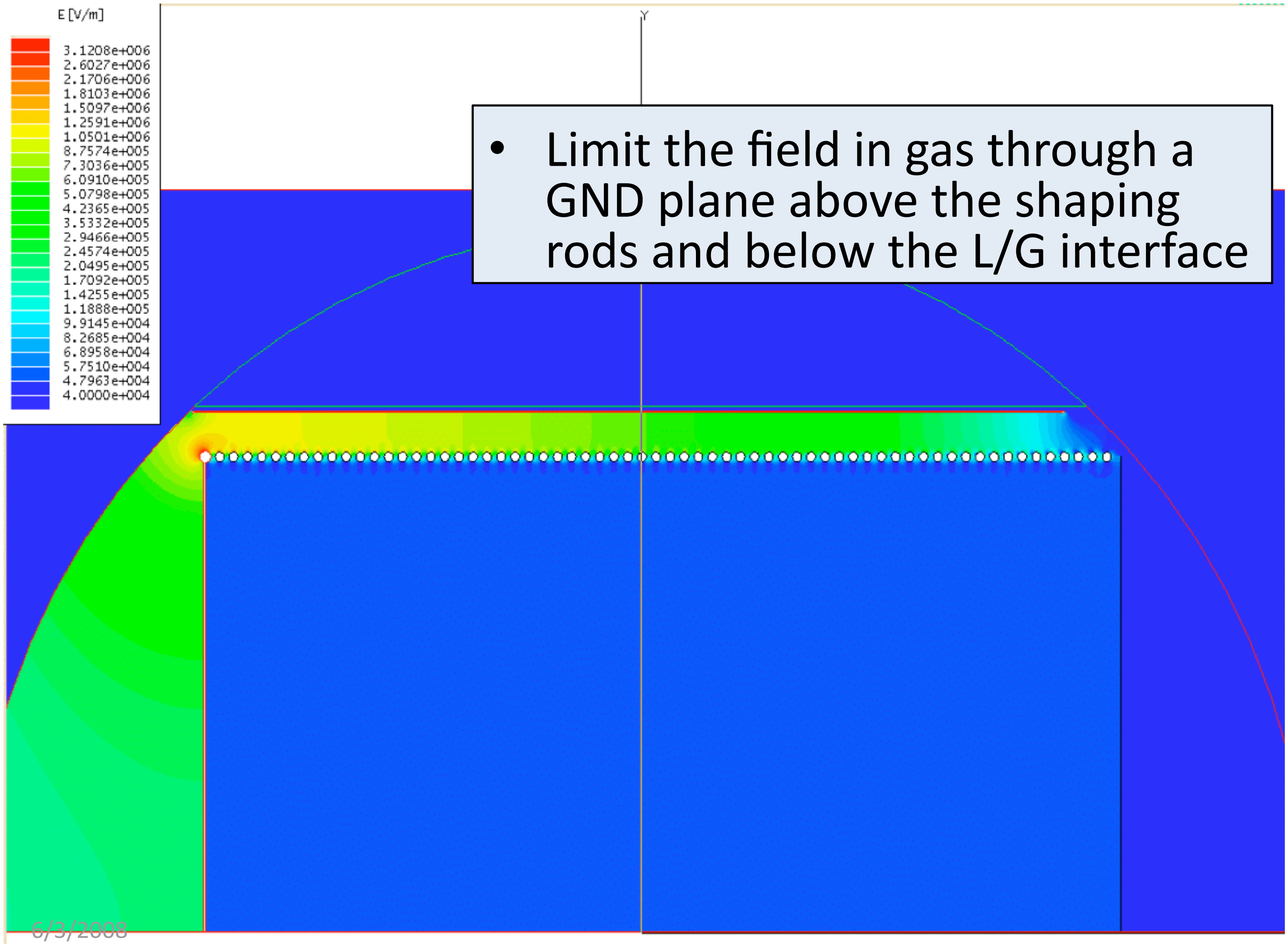
Phase-I: Field Shape/Optimization



Nominal Drift Field 500V/cm
HV=-125kV

Max. vertical component along 2 lines of drift 10 and 25 cm away from the shaping rods

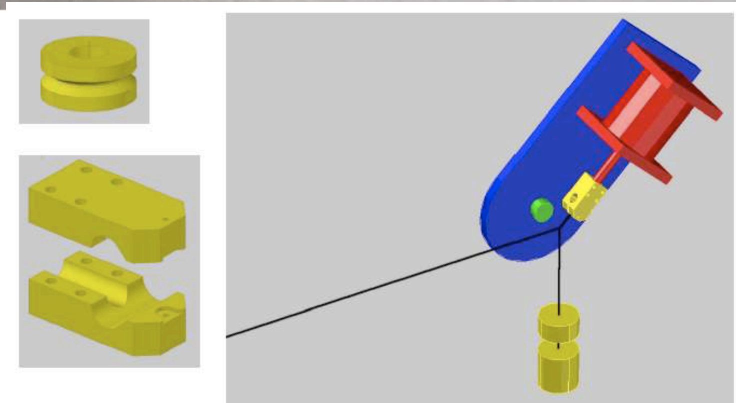
Phase-I: Field Shape/Optimization



- Limit the field in gas through a GND plane above the shaping rods and below the L/G interface

Phase-I: Wire properties

- Wire Properties
- Wire termination
  - Robustness up to 3kg tension
  - Conceptual winding machine

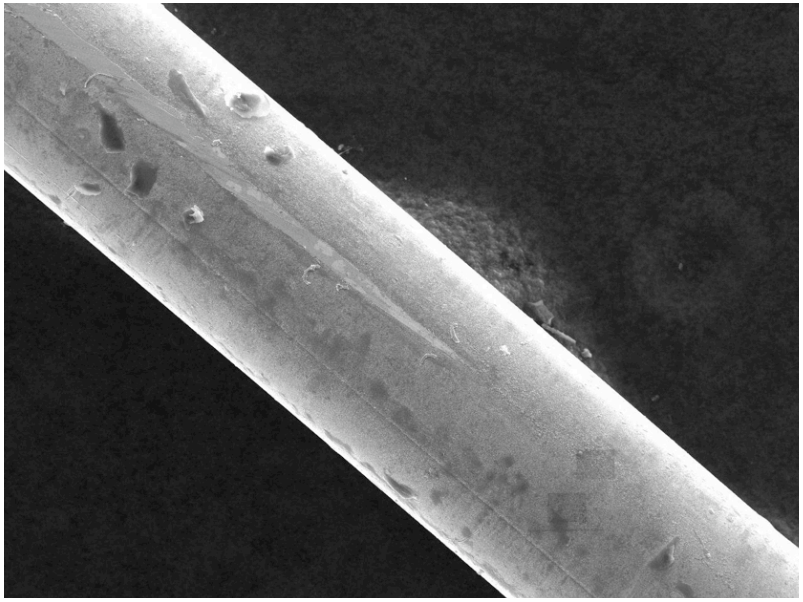


	SS304V (Fort Wayne)	CuBe (Little Falls Alloy)
Young's modulus @ RT	170GPa	121GPa
Young's modulus @ LN2	183GPa (8% increase)	136GPa (12% increase)
Integral CTE	0.22%	0.29%
Tension increase due to cooling	~750g	~730g
Max. tension with termination	~3kg	~2kg

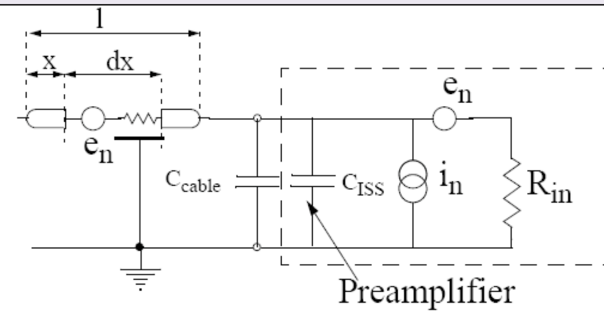
- 1kg tension -> 7mm (on a 2.5m long wire)
- Wire shrinkage if suddenly at T=90K : 6.8mm (while the frame kept at RT)
- Nominal tension ~1kg

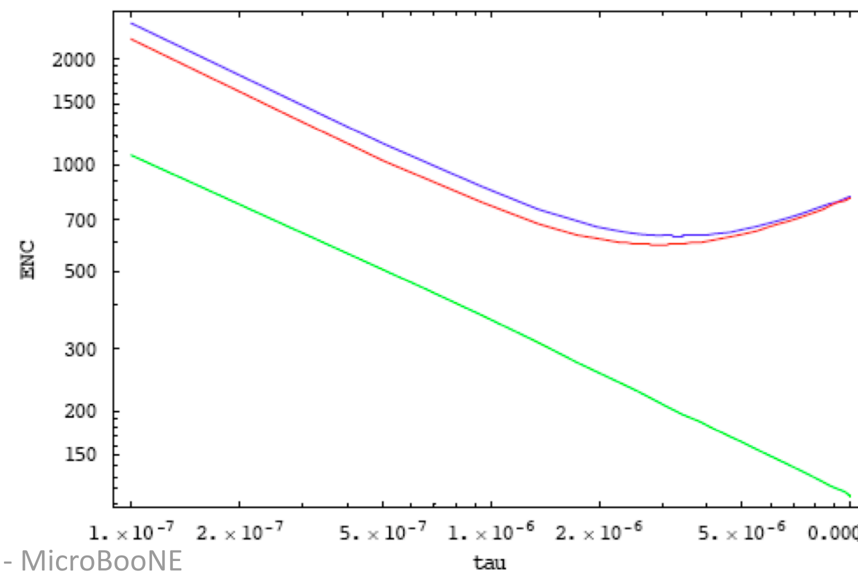
- Max. sagging (5m long wire): 0.45mm
- Max. Sagging vs. tension ~50um/N (at 10N)
- 10% tolerance on wire tension results in 50um variations on sagging

Phase-I: Wire Plating

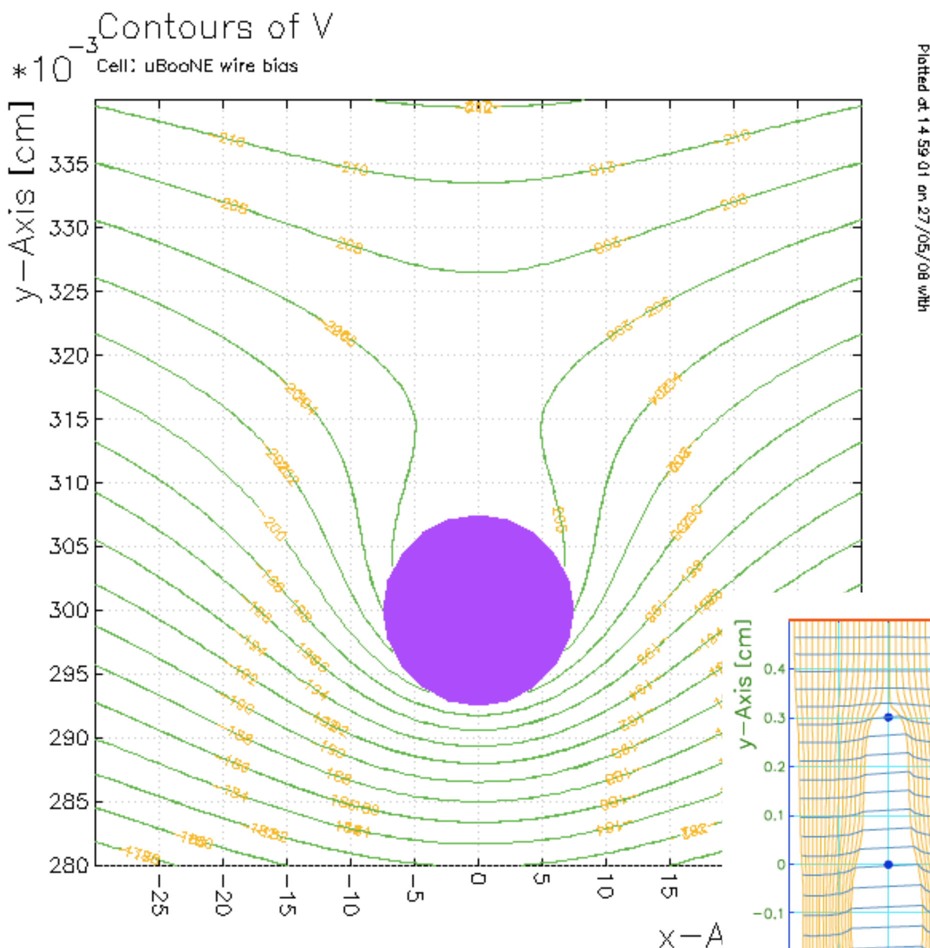


- Equivalent Noise Resistance of a low noise preamplifier is 10Ohm
- Needs low resistivity metal wires or plating
- SS plated analysis at elec. Microscope to identify inconsistencies in R





Phase-I: Wire Bias

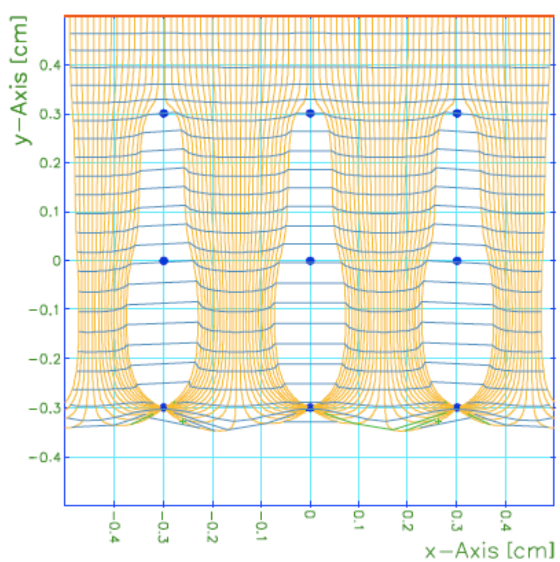


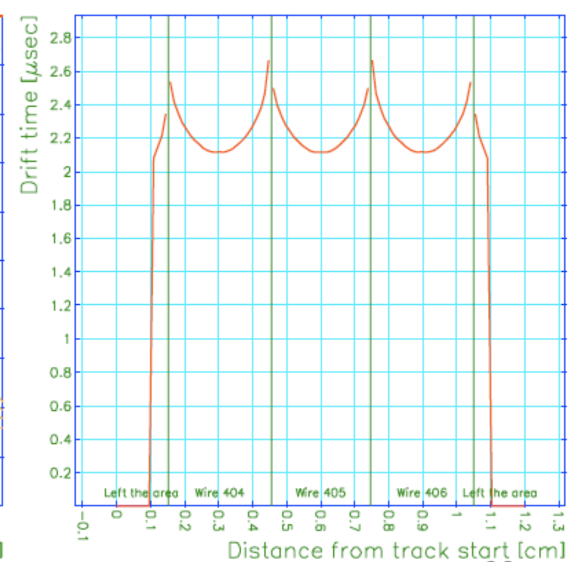
- 3 wire planes act as electrostatic grid
- Full transparency condition:

$$\frac{E_2}{E_1} \geq \frac{1+\rho}{1-\rho} \quad > 1.37 \qquad \rho = \frac{2\pi r}{d}$$

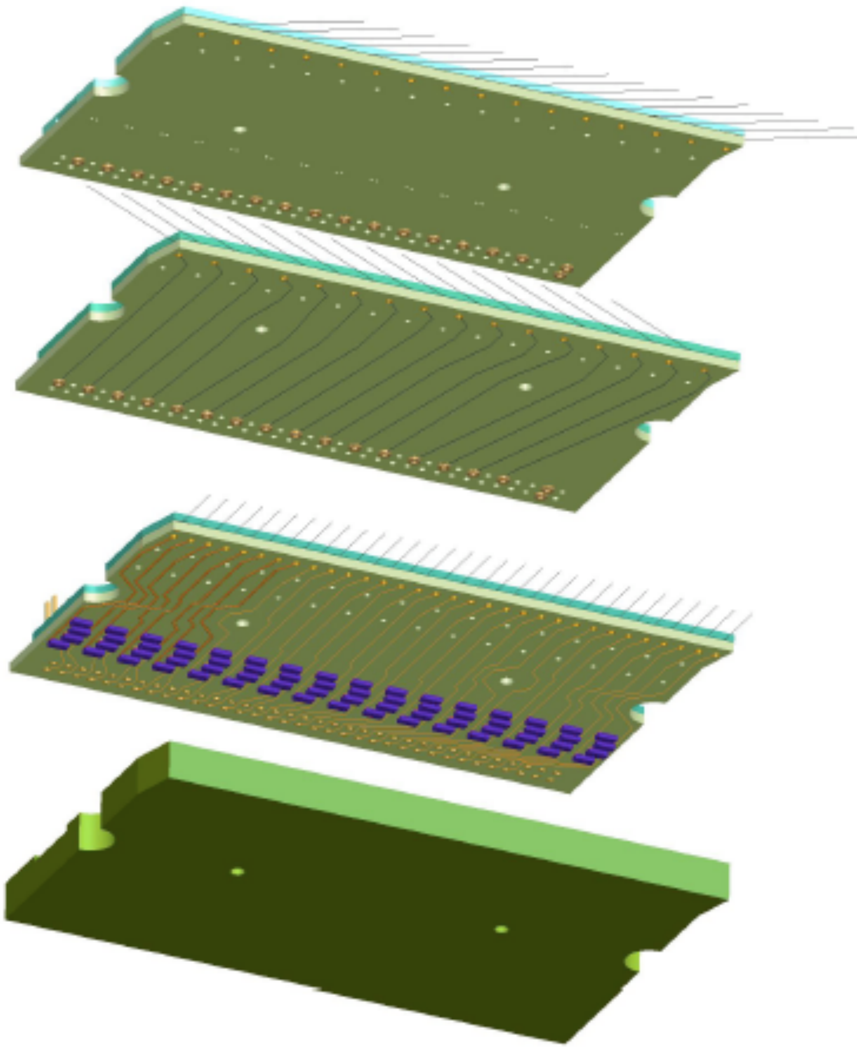
r=0.15mm
d=3mm

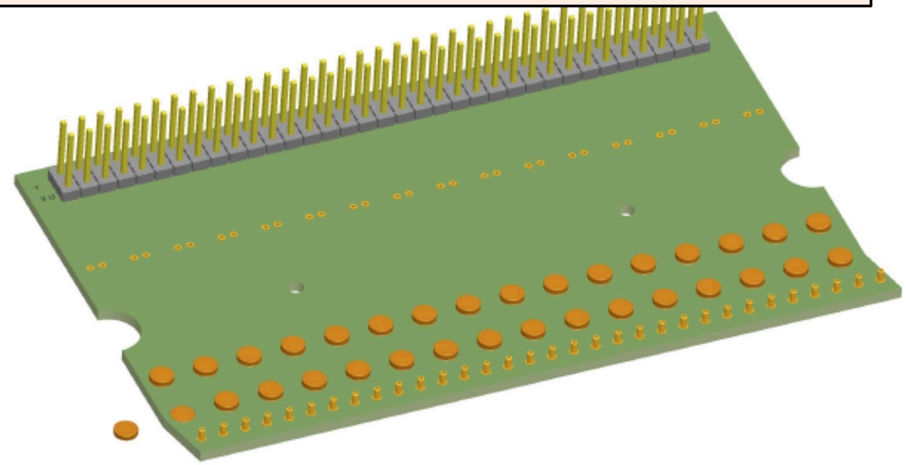
V1 = -205V
V2 = 0V
V3 = 440V

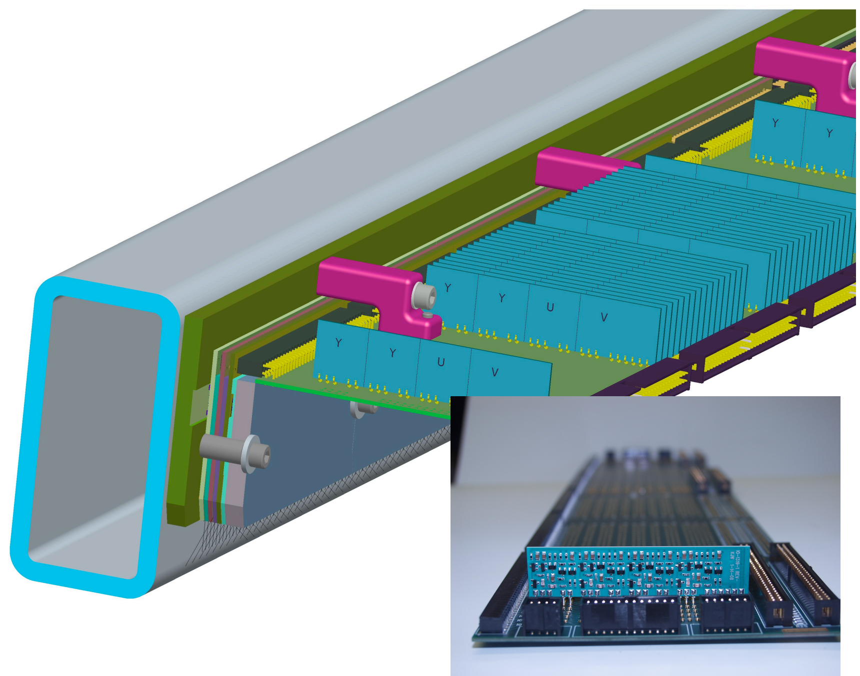




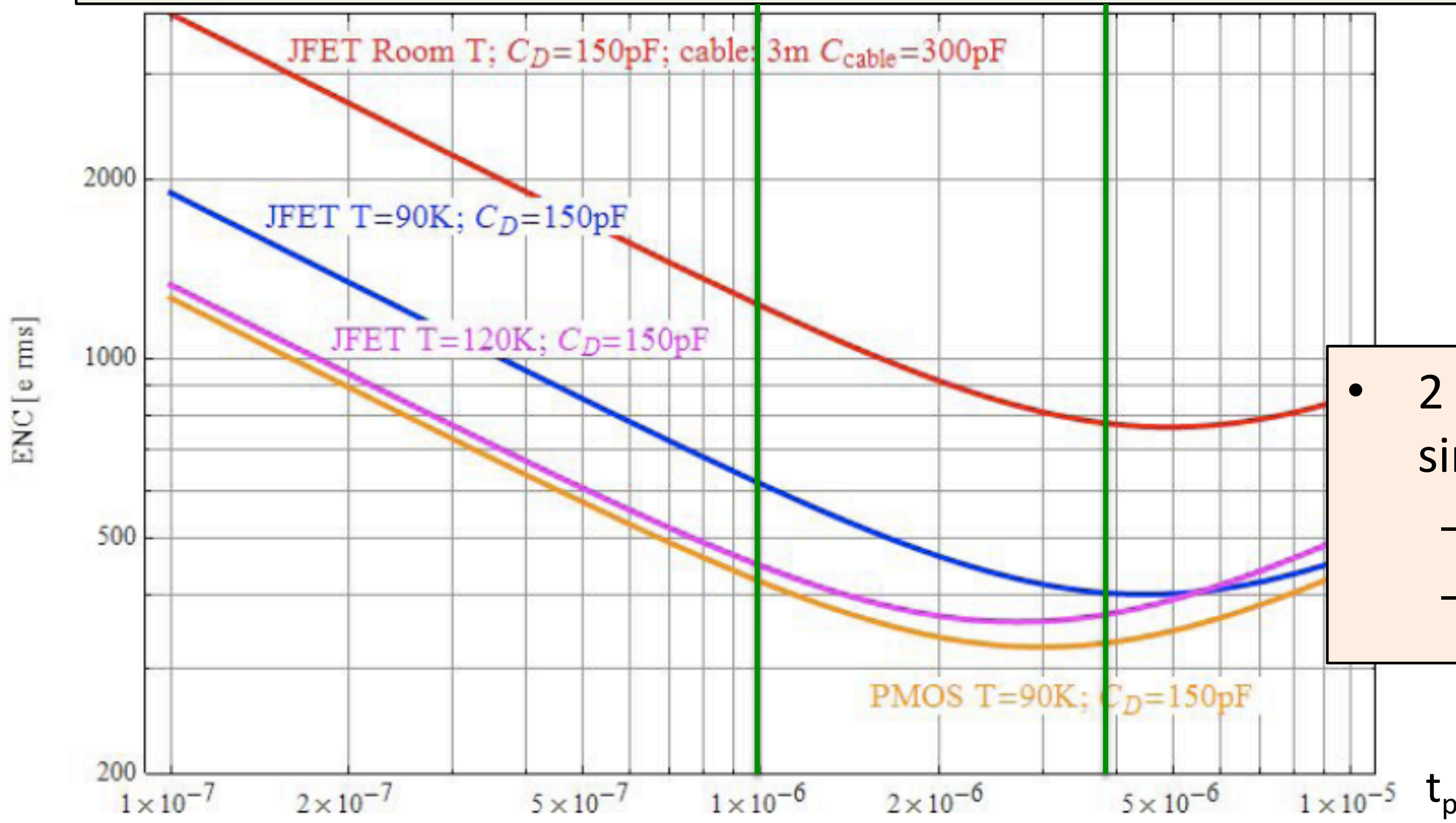
Phase-I: Wire Connections







Readout Electronics

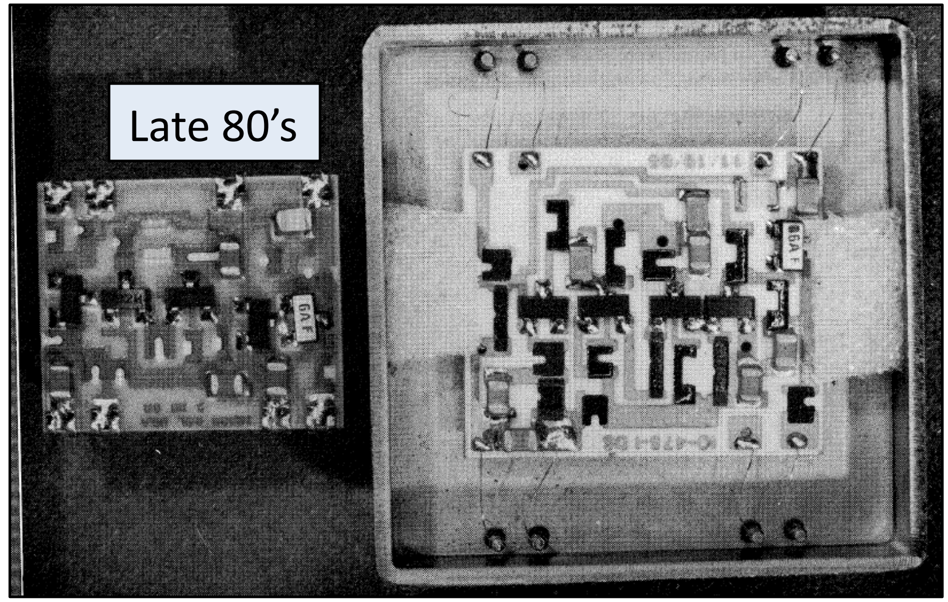


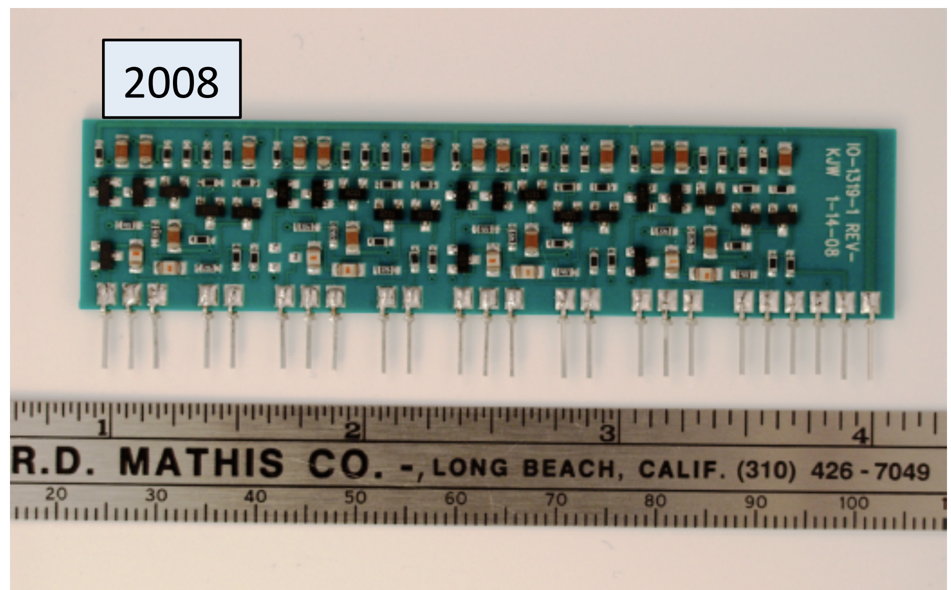
- 2 technologies with similar performance
  - JFET @ T=120K
  - pMOS @ T=90K

- Best performance (i.e. S/N) achievable reducing the capacitive load seen at the preamplifier input
  - Place the front-end as close as possible to the wire minimizing the connection lengths
  - Cold electronics: performance optimized at cryogenic temperature
  - Factor ~3 at least better than at room temperature
- For energy and position measurements optimal shaping in the range 0.5-2μs
  - Parallel noise sources (disturbances on HV, wire bias, microphonic)

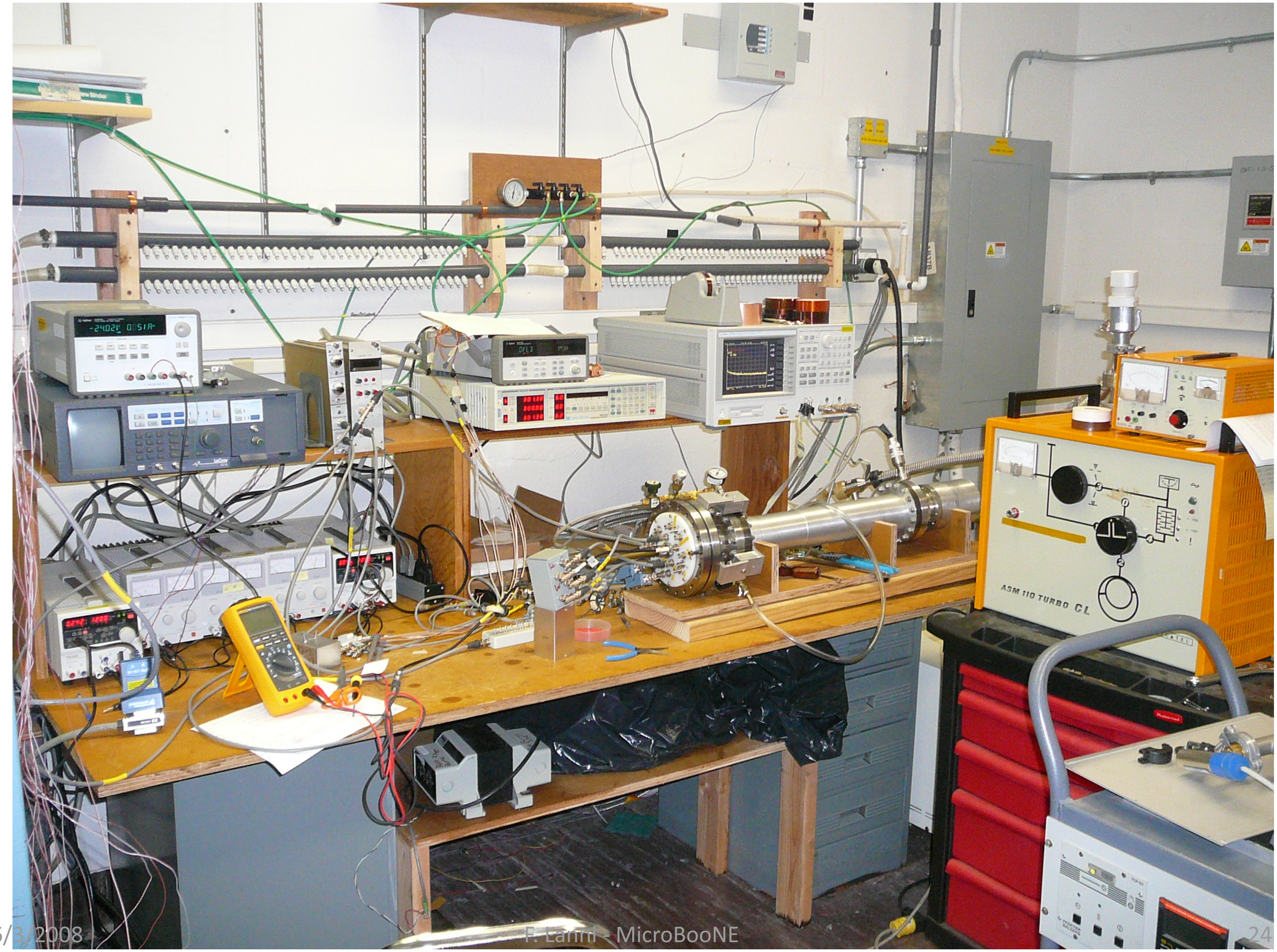
Cryogenic Front-End based on on JFET

- Technology mature and available as of today
  - Reliability issues requires a careful choice of component and high-reliability assembly
  - Ceramic hybrid with co-fired traces and surface mount components properly tested
- Several years of experience
- Helios-NA34:
  - 576 preamplifiers
  - Operations: 4 years, multiple cool-downs
  - Failure: 1
- NA48:
  - Preamplifiers in LAr: 13,000
  - Operated at very high voltage
  - Failures: ~50 because of a HV accident in 1998. Negligible failures after that
  - Always kept at cryogenic temperature
- Contamination issues: see Stephen plot w. microBooNE prototype

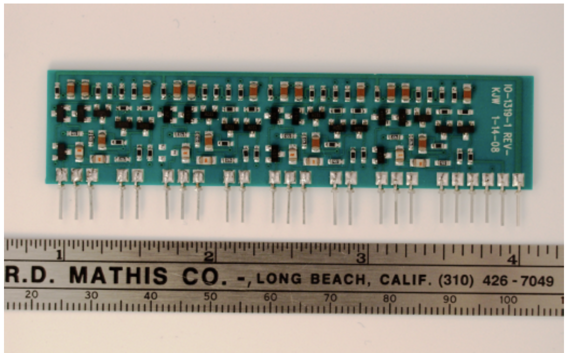




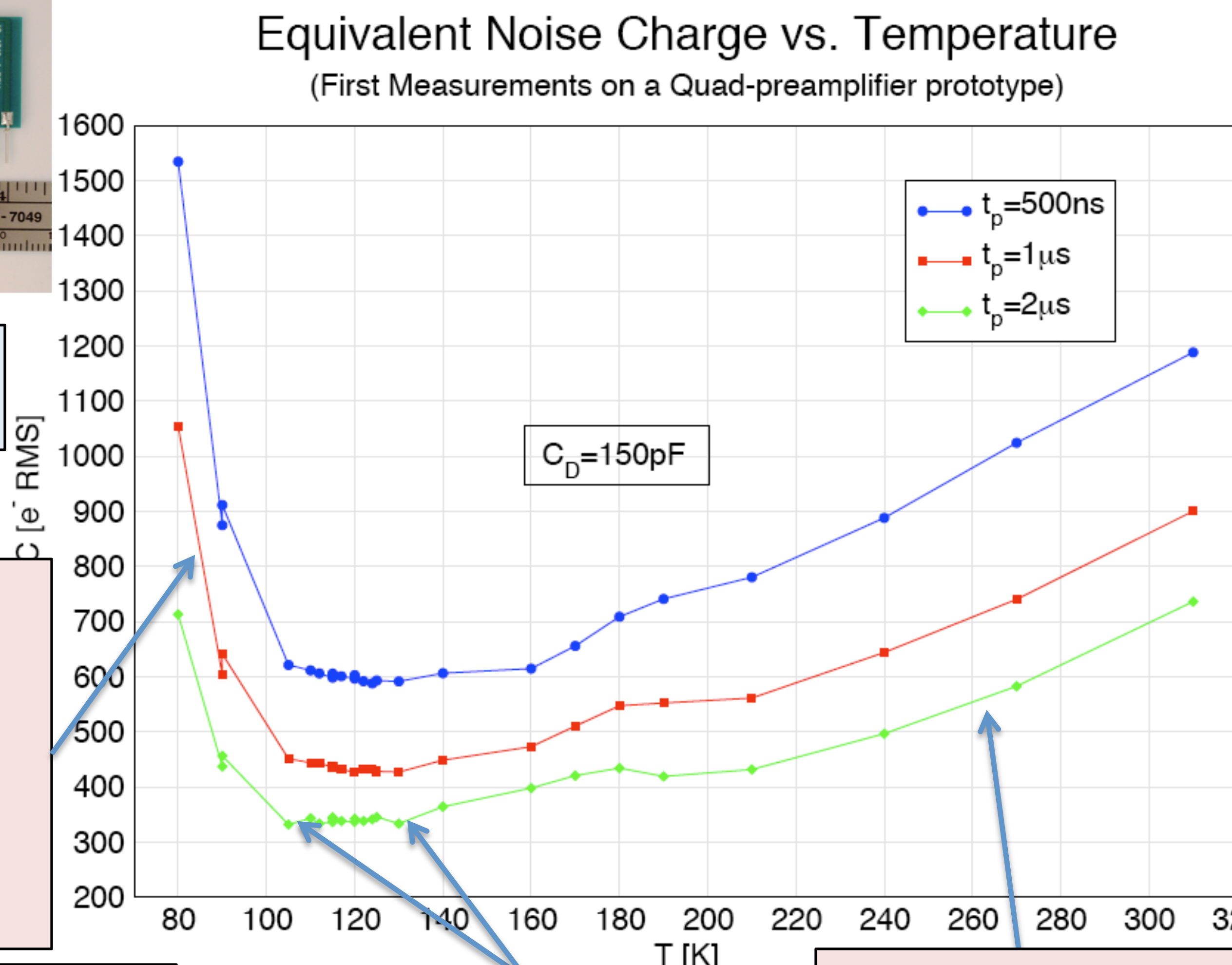
Cryogenic Electronics Setup



JFET Preamplifier Noise



In JFETs majority carriers in the channel are electrons



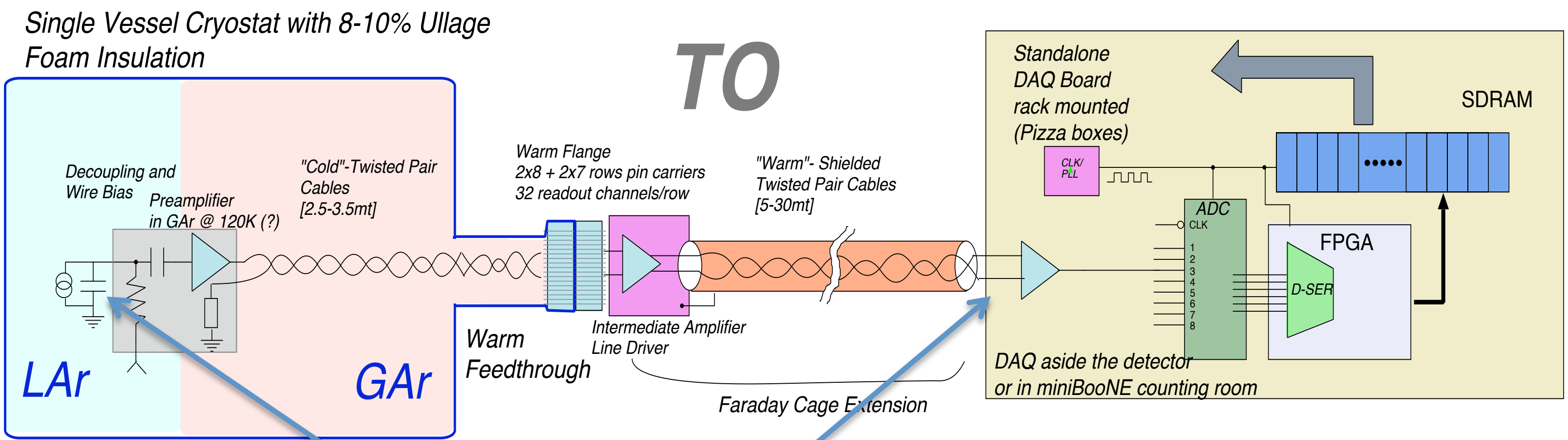
Electron freeze-out:
Donor levels are ~40-50mV below band conduction, so a further reduction of temperature causes more and more electrons to fall in their donor energy levels.

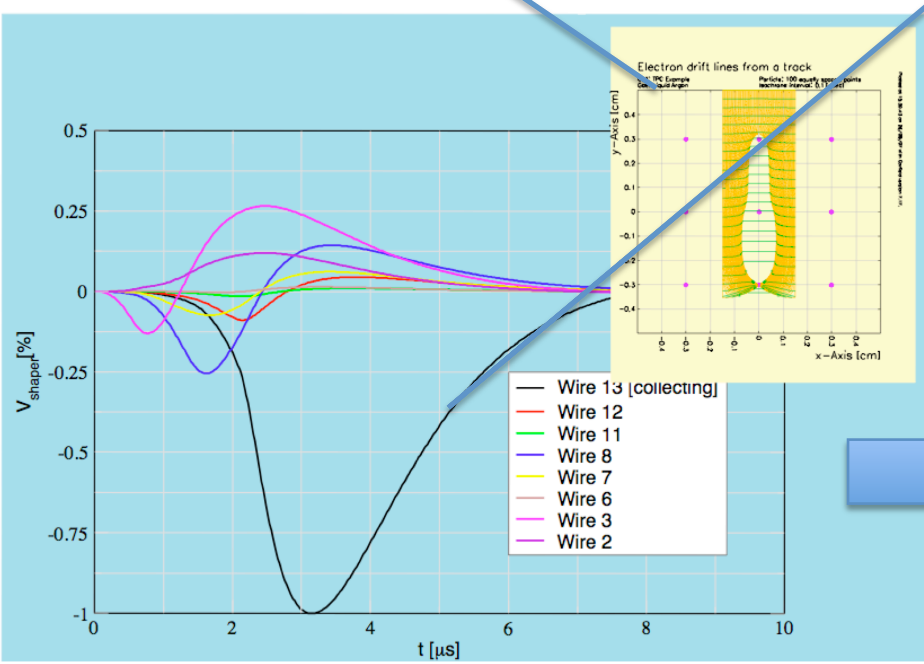
In CMOS the conducting channel in Enhancement mode is formed by inversion (energy band bending at the Si/SiO2 interfaces)

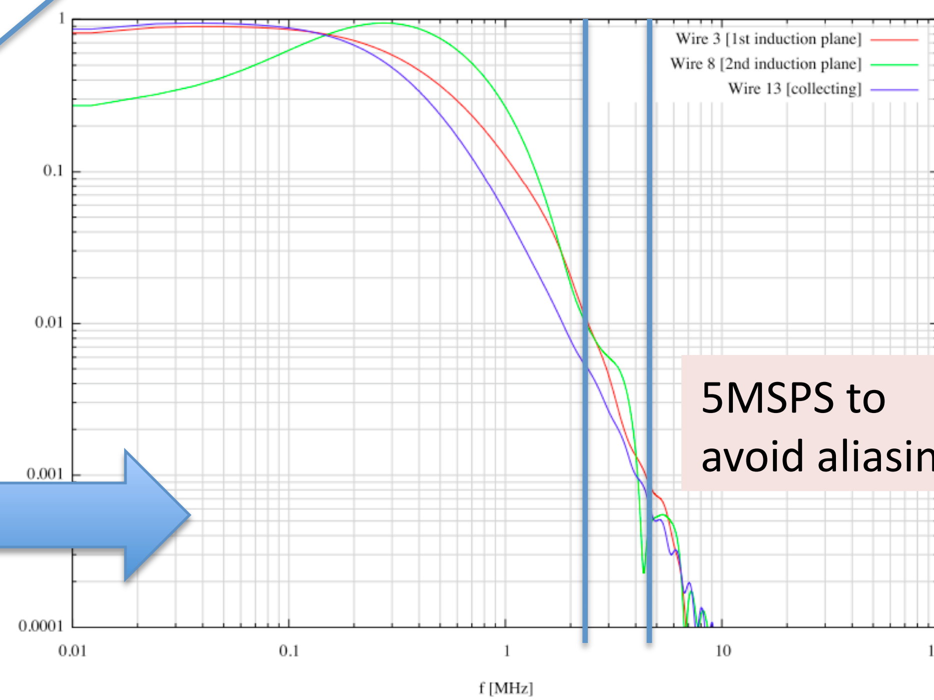
At high doping concentrations mobility increases and reaches a max., then decreasesdue to impurity scatteringas the temperature of the lattice is reduced compared to the electron temperature

Bulk mobility increases as temperature is reduced. Transconductance also.

MicroBooNE Readout: Shaping, Sampling Time and DAQ

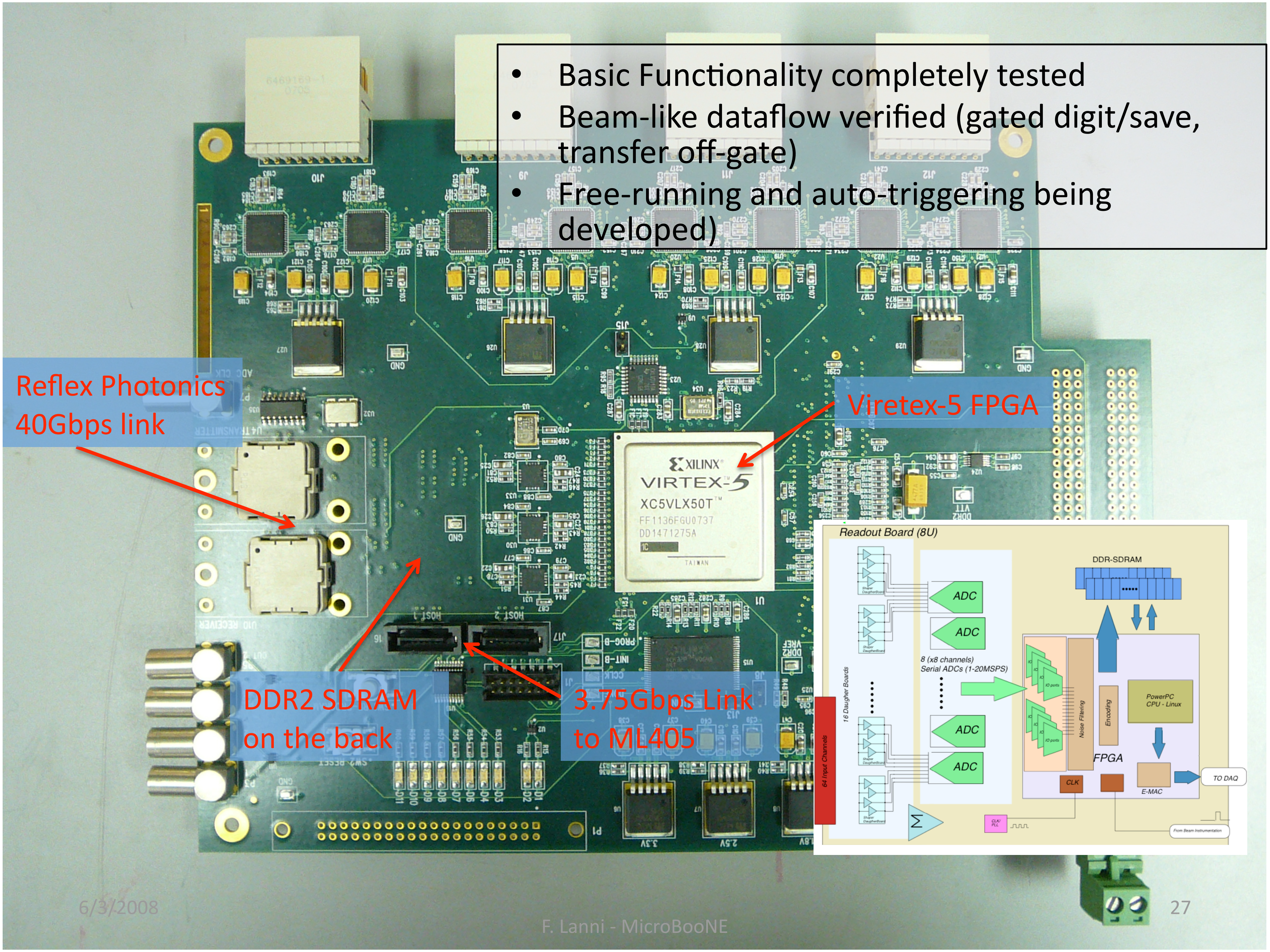






5MSPS to avoid aliasing

- Basic Functionality completely tested
- Beam-like dataflow verified (gated digit/save, transfer off-gate)
- Free-running and auto-triggering being developed)

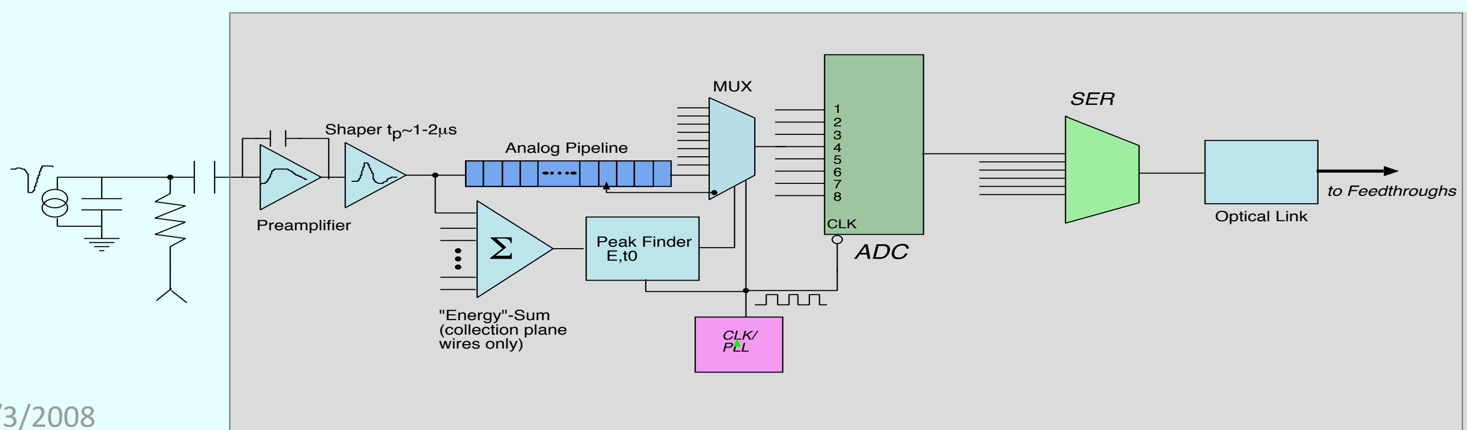


Phase II: R&D on Readout for large scale detectors

- Readout optimization for large scale detectors (20-100ktons) has to go hand in hand with design of the overall detector.
- Most of the issues presented for microBooNE have to be reconsidered for scaling up
  - Wire Length: up to 8-10max in Y, 16-20 in U/V
  - Geometry (i.e. pitch and distance)
  - S/N (related to length, pitch and wire's plane distances)
  - Mechanical issues
  - Drift length (5mt?)
    - Purification issues
    - Diffusion?
- Feedback of real data analysis from microBooNE will allow to optimize some of the functional blocks of any readout architecture for a scaled up detector. Particularly:
  - Optimal Shaping (0.5us – 2us)
  - Sampling
  - Dynamic Range
  - Storage, data volume
  - Data Transmission
  - POWER!!!

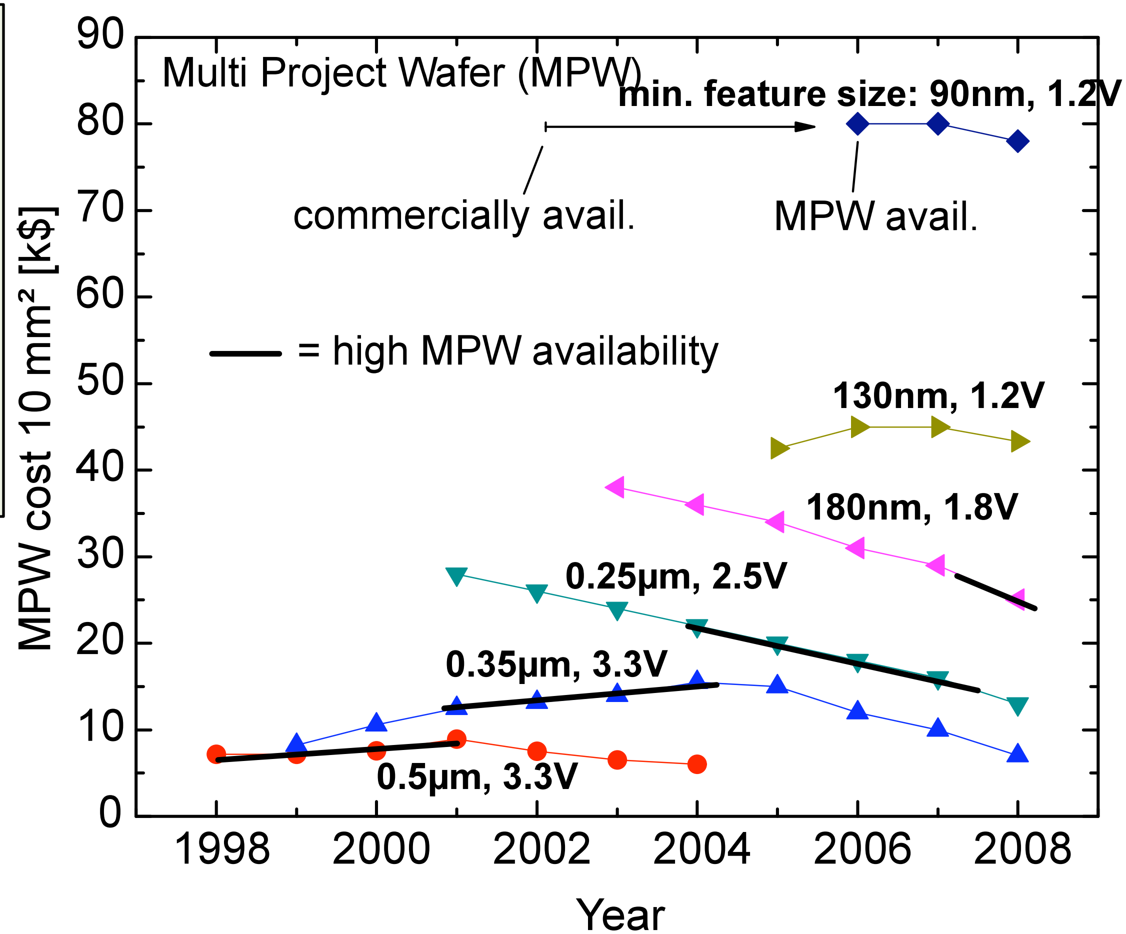
Phase II: Readout (cont.)

- For S/N optimization we want to study an architecture operating as close to the detector, i.e. at T=87K
  - JFET technologies is NOT suitable because it doesn't give flexibility in the detector geometry optimization>
  - Particularly as far as modularity and assemblying of several modules in a single vessels (see David talk)
  - CMOS technology with a low-noise pMOS input transistor
- Other issues are related to minimize the number of penetrations in the vessel in the process of simplify the overall detector design particularly in terms of:
  - Cables
  - Feedthroughs
  - Heat Load
- Fully integrated ASIC R&D based on CMOS technology
- Architecture has to include functionalities that are sketched here



Phase II: Readout (cont.)

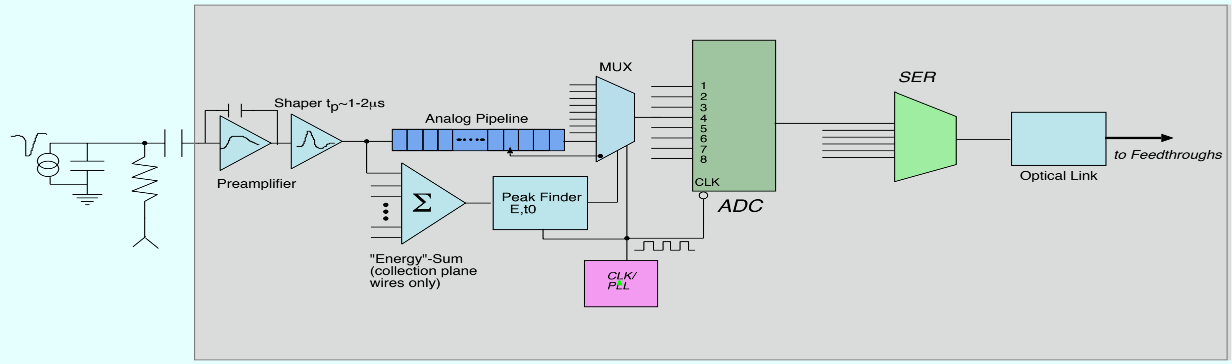
- To plan such an R&D we need to understand what process (i.e. feature sizes) will be suitable by the time the application will demand it
  - Electronics is evolving fast



- Costs increase significantly w. reduction in feature size
- For cost effectiveness HEP and NP projects fit into MPW fabs
- MPW spans ~4-5 years
- Foundries maintain technology for several years after end of MPW
- Lifetime 10-15 years

Fan application whose production will be around ~2015 probably we will have to consider or target like 180nm.

Phase II: Readout (cont.)



- Literature shows suitability of CMOS processes (0.5 and 0.35um) at cryogenic temperatures
- However smaller feature sizes are significantly different processes.
- An example are the way metallization layers are grown (which also scale down).
- Thermal stresses can induce failures of the devices.
- Portability from one technology to the other in terms of behaviour at cryogenic temperatures is not straightforward

- Also the implementation of the functional blocks sketched above would require an architecture radically different from what traditionally used in our field.
  - Design portability
  - Current-mode architecture

Phase II: Readout (cont.)

- An R&D for a fully integrated low noise, low power and multi-function ASIC intended for scaled detector would require approximately 4 years
  - From start up to be ready for production
  - Not without risks associated

1. Investigate technologies and develop models for cryogenic operations

   6 months: up to end of 2008

2. Characterize analog & mixed-signals ASIC already developed towards cryogenic operations:

   3 months

3. Select Technology and develop test structures and sub-circuit (analog and digital): 2-3 fabs

   18 months: beg 2009 / mid 2010

4. Develop readout architecture (charge amplification in current-mode, processing, sampling, storage, multiplexing….)

   3 months

5. Develop ASIC (might be in functional blocks: low-noise, low-power analog, mixed signal readout): 2-3 fabs

   24 months: mid 2010 / mid 2012

Conclusions: Technical scaling issues in microBooNE

- MicroBooNE in our view IS the proper (70 ton fiducial) first step – as full running experiment – in a U.S. LAr TPC R&D program toward massive (>20kton) detectors
- The ability to tag $e/\gamma/\pi^o$, low sensitivity and high resolutions allow for unique measurements needed to understand the sensitivity of LAr detectors for long baseline experiments
  - Size reduction can compromise those measurements
- Transversal dimensions maximized compatibly with off-site construction and transport
  - **Critical for aiming at large volume detectors with drift of 4-5mt**
- Overall size (170 ton total volume) needed to test ability of purification system to achieve and maintain purity in the detector.
- Electronics R&D scaling issues need to be on a parallel path because of technology requirements and time needed for development assessment.
- However microBooNE is provided with the same S/N (that will be used in the large scale detectors) to explore the physics cases and goals

Backup Slides

Phase-I: Cryostat